Ozy - Jumpers and Connectors

Connector/ Jumper	No. pins	Signal/Destination	default		optional
J8	9	FPGA_GPIO 13….16+22…24	PTT/KEY	5=GND, 6=Dash, 7=DOT/PTT	
J20	25	Parallel Port to SDR1000		J20/1-17 used /18-25 on GND on SDR-PIO	
P1		USB	USB cable to PC		
J32	3	+5V USB	Jumper 1-2	+5VBUS to Regulator U14 (3.3V)	n.b.
J26	3	+3.3V from Atlas-BUS or regulator onboard	0R0 1-3	+3.3V from U14 is used on board	Jumper 1-2 (3,3V from Atlas/U14 n.b.)
J1	2	Ext. RX-CLK in (CLK3, LVDS)	n.c.		
J2	2	Ext. RX-CLK in (CLK2, LVDS)	n.c.		
J3	2	Ext. TX-CLK out (CLKX, LVDS)	n.c.		
J4	2	Ext. TX-CLK out (CLKY, LVDS)	n.c.		
J12	2	RE~=0 SN65LVDM050D	n.c.	Ext. LVDS CLK Receive Enabled	
J13	2	DE=+3.3V SN65LVDM050D	n.c.	Ext. LVDS CLK Transmit Enabled	
J10	2	FPGA_CLKXOUT-FPGA_CLK4IN	0R0		
J11	2	FPGA_CLKYOUT-FPGA_CLK5IN	0R0		
J5	2	I2C EXT	n.c.		
J6	10	RS232 EXT (from/to MAX 1406)	n.c.		
J7	2	EXT RESET	n.c.		
J9	3	data from J8 via ULN2003 or direct to FPGA	0R0 1-3	J8/1-ULN2003-FPGA_GPIO13	
J16	3	data from J8 via ULN2003 or direct to FPGA	0R0 1-3	J8/2-ULN2003-FPGA_GPIO14	
J18	3	data from J8 via ULN2003 or direct to FPGA	0R0 1-3	J8/3-ULN2003-FPGA_GPIO15	
J19	3	data from J8 via ULN2003 or direct to FPGA	0R0 1-3	J8/4-ULN2003-FPGA_GPIO16	
J22	3		0R0 1-3	J8/9-ULN2003-COM	
HDR1	10	Active Serial	n.c.	AS Programming Header	
HDR2	10	JTAG	n.c.	JTAG Programming Header	
J17	20	FPGA_GPIO 1…17	n.c.		
J25	2	OE=0 for FPGA_GPIO 17…24 to J17	0R0	Data from J20/10...13+15 and J8/6…8 connected to FPGA_GPIO17…24	
J30	2	OE=0 for FPGA_GPIO 1…8 to J20/2…9	n.c.	FPGA_GPIO 1…8 NOT connected to J20/2…9	
J21	2	FPGA_CLK6IN, FPGA_CLK7IN	n.c.	Optional Clocks	
J23	3	FPGA_MSEL1	Jumper 2-3	MSEL1=0 Passive Serial	
J24	3	FPGA_MSEL0	Jumper 1-2	MSEL2=1 Passive Serial	
J27	2	I2C (SDA) connection to Atlas_A21	0R0	I2C (SDA) connected to Atlas_A21	
J28	2	I2C (SCL) connection to Atlas_A20	0R0	I2C (SCL) connected to Atlas_A20	
J29	2	Reset Line to ATLAS X17C1	n.c.	Reset Line connected to ATLAS X17C1	